REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-18 are now present in this application. Claims 1, 8, 14, 17 and 18 are independent.

Claims 1, 8-9 and 14-16 have been amended. Claims 17 and 18 have been added. Reconsideration of this application, as amended, is respectfully requested.

Priority Under 35 U.S.C. § 119

Applicants thank the Examiner for acknowledging Applicants' claim for foreign priority under 35 U.S.C. § 119, and receipt of the certified priority document.

Drawings

The Office Action indicates that the drawings are accepted by the Examiner. However, Applicants have not received a Notice of Draftsperson's Patent Drawing Review PTO-948 or other indication of whether or not the formal drawings have been approved by the Draftsperson. Since no objection has been received, Applicants assume that the drawings are acceptable and

that no further action is necessary. Confirmation thereof in the next Office Action is respectfully requested.

Objection to the Oath/Declaration

The Examiner has objected to the oath/declaration asserting that the oath or declaration does not identify this application by the application number and filing date and does not identity the citizenships of each inventor.

The Applicants respectfully submit that pursuant to a Notice of Informal Application dated January 31, 2002, a Substitute Declaration was filed. A copy of the Notice of Informal Application, Substitute Declaration and filing receipt are enclosed. It is requested that these be made part of the record.

Accordingly, reconsideration and withdrawal of this objection are respectfully requested.

Objection to the Drawings

The Examiner has objected to the drawings, asserting that according to Fig. 3, the base-emitter junction of a bipolar transistor B1 as well as a gate-source of the NMOS transistor is short-circuited and therefore none of the transistors can be controlled by an external signal, such as a current flow through the diodes. The Applicants respectfully disagree.

As the Applicants have provided, if the 0.7V potential barrier between the n+ source region and the p+ substrate is overcome, the transistor B1 is turned on. The voltage required to overcome this barrier is referred to as the "triggering voltage". The device of the background art required a stress voltage of at least 7 volts to be applied to the drain in order to overcome the barrier potential between the n+ source region and the p+ substrate. As alluded to by the Applicants, substrate resistance determines the on/off state of the protection device by providing current discharge paths from *drain to substrate* and *drain to source*. In other words, if a high voltage i.e., 7 volts is applied to the drain, holes are discharged to the substrate by junction breakdown between the n+ source region and the p+ substrate (Applicants' original specification, paragraph 9). Thus, discharge paths are provided.

In the device shown in Fig. 3, while it appears that that various leads of the respective transistors are shorted, current flow does not occur until the barrier potential of the internal junctions are overcome by a certain level of voltage. In other words, the devices are not shorted until they are turned on (and they are not turned on until the barrier potential is exceeded). Keeping in mind that while the stress voltages appearing at the node B are transient voltages, they do have a high value momentarily, despite the direct connection to ground. Thus, a high voltage, momentarily applied at node B, increases the potential of the substrate. When the potential of the substrate becomes high, a

voltage drop (for example, 0.7V) occurs with ease between the source of B1 and the substrate. Thus, transistor B1 is triggered at a lower voltage, and discharge paths are provided for the stress voltage appearing at the drain (see Applicants' specification, paragraph 28).

Reconsideration and withdrawal of this objection to the drawings is respectfully requested.

Rejection Under 35 U.S.C. § 102

Claims 1 and 3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Avery. This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the instant application, Applicants respectfully submit that independent claim 1 has been amended to recite a combination of elements in an electrostatic discharge (ESD) protection circuit, including at least one diode connected between the input/output pad and the NMOS transistor, a cathode of said at least one diode being connected to the ground.

Applicants respectfully submit that this combination of elements as set forth in independent claim 1 is not disclosed or made obvious by the prior art of record, including, Avery.

Particularly, Avery does not disclose a diode having a cathode thereof connected to ground. Therefore Avery fails to teach a combination of elements in an electrostatic discharge (ESD) protection circuit, including at least one diode connected between the input/output pad and the NMOS transistor, a cathode of said at least one diode being connected to the ground, as recited in independent claim 1, as amended. Menon cannot supply the deficiency of Avery.

Claim 3 depends on claim 1, and therefore is patentable at least for the reasons stated with respect to independent claim 1. Reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

Rejections under 35 U.S.C. §103

Claims 2, 4, 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Avery in view of Menon. This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

Avery, argued above, fails to disclose a combination of elements in an electrostatic discharge (ESD) protection circuit, including at least one diode connected between the input/output pad and the NMOS transistor, a cathode of said at least one diode being connected to the ground.

Menon discloses a series of diode-connected transistors 40. In such a configuration, the emitter of the transistor is regarded as the cathode of a diode. While Menon provides that the diode-connected transistors are referenced to ground potential, Menon does not disclose a diode or diode-connected transistor having a cathode thereof actually connected to ground. The Examiner also recognizes that any point in a circuit can be *referenced to ground* without being connected thereto. Menon does not disclose the recited connectivity.

Therefore, Menon, like Avery, fails to disclose or suggest a combination of elements in an electrostatic discharge (ESD) protection circuit, including at least one diode connected between the input/output pad and the NMOS transistor, a cathode of said at least one diode being connected to the ground, as recited in independent claim 1, as amended.

Claims 2-7 depend, either directly or indirectly on independent claim 1, which is believed to be allowable, and are therefore claims 2-7 are allowable based on their dependence from claim 1. Reconsideration of this art grounds of rejection is respectfully requested.

Claims 8 and 10-13

The Examiner has not provided specific art grounds of rejection for claims 8 and 10-13. However, claim 8 has been amended to recite a combination of elements in an electrostatic discharge (ESD) protection circuit, including the NMOS transistor is connected between the input/output pad and has a parasitic bipolar transistor connected to the plurality of N diodes, the cathode of at least one of said plurality of N diodes being connected to a ground. Applicants respectfully submit that this combination of elements as set forth in independent claim 8 is not disclosed or made obvious by the prior art of record, including, Avery and Menon, argued above.

Claims 10-13 depend, either directly or indirectly on claim 8, and are therefore claims 10-13 are allowable based on their dependence from claim 8, which is believed to be allowable. Reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Avery in view of Menon, and further in view of Duvvury. This rejection is respectfully traversed.

While not conceding to the appropriateness of the Examiner's rejection, Applicants respectfully submit that claim 14 has been amended to recite a combination of elements in an electrostatic discharge (ESD) protection circuit, including the NMOS transistor is connected between the input/output pad and

has a parasitic bipolar transistor connected to the plurality of N diodes, the cathode of said diodes being connected to a ground. Applicants respectfully submit that this combination of elements as set forth in independent claim 14 is not disclosed or made obvious by the prior art of record, including, Avery and Menon, argued above. Duvvury does not teach a diode having a cathode thereof connected to ground, and therefore cannot supply the deficiencies of Avery and Menon. Reconsideration and withdrawal of this art grounds of rejection is respectfully requested.

Claim 16 depends on claim 14, which is believed to be allowable, and therefore claim 16 is allowable based on its dependence from claim 14. Reconsideration and allowance thereof is respectfully requested.

Allowable Subject Matter

The Examiner states that claims 9 and 15 would be allowable if rewritten in independent for including all of the limitations of the base claim, and any intervening claims.

Applicants thank the Examiner for the early indication of allowable subject matter in this application. Claims 9 and 15 have been rewritten in independent form as new claims 17 and 18, which therefore should be allowable.

Additional Cited References

Since the remaining references cited by the Examiner have not been utilized to reject the claims, but have merely been cited to show the state of the art, no comment need be made with respect thereto.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) respectfully petition(s) for a two (2) month extension of time for filing a reply in connection with the present application, and the required fee of $420.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachments: Copy of Notice of Information Application
Copy of Substitute Declaration
Copy of Official Filing Receipt